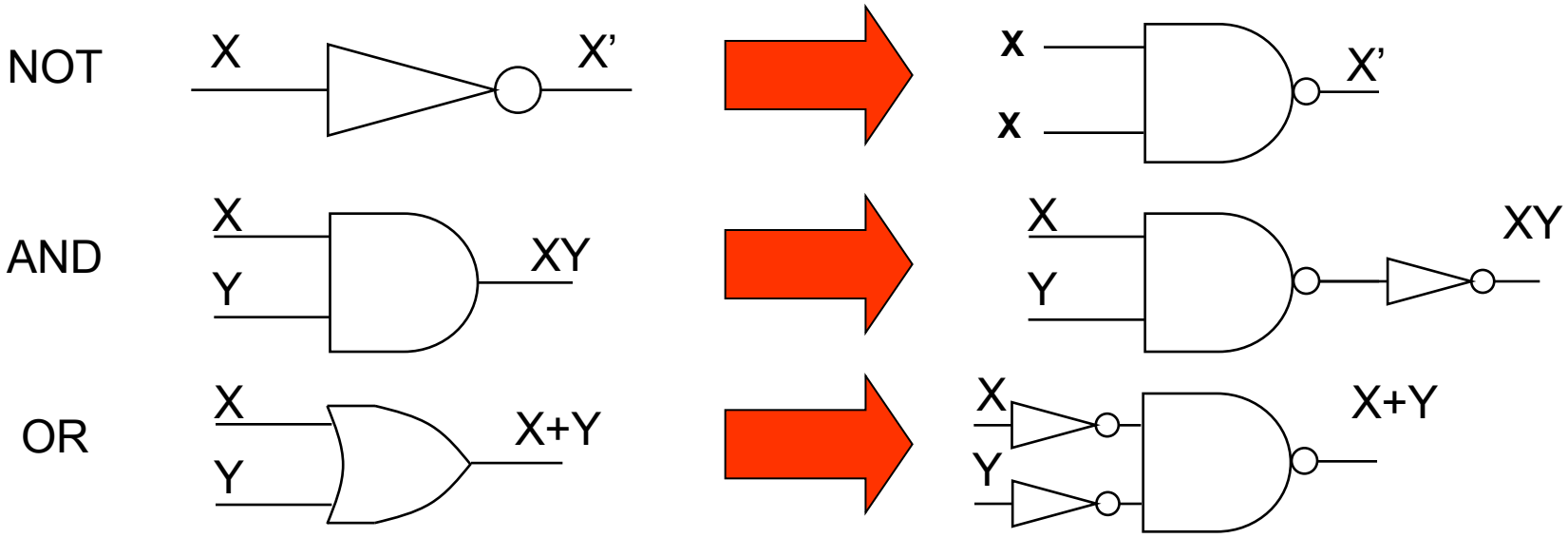
Implementation using NAND and NOR Gates

Combinational Logic

NAND Gate is Universal

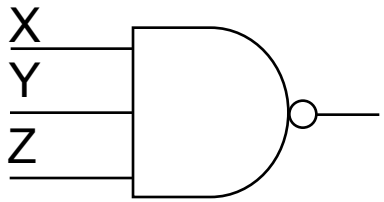


- Therefore, we can build all functions we learned so far using NAND gates ONLY *(Exercise: Prove that NOT can be built with NAND)*
- NAND is a UNIVERSAL gate

Graphic Symbols for NAND Gate

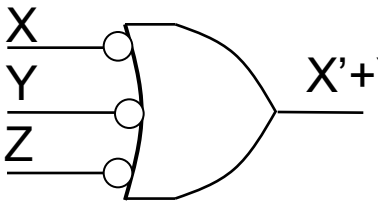
Two equivalent graphic symbols or shapes for the SAME function

AND-NOT



(XYZ)’

NOT-OR

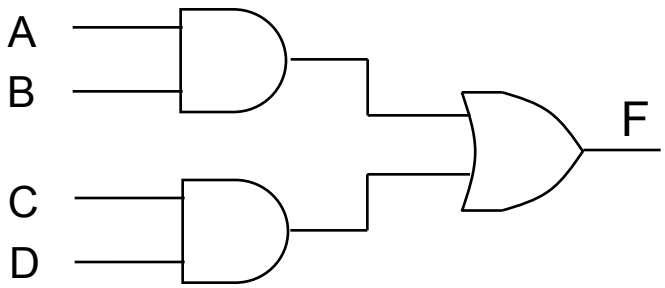


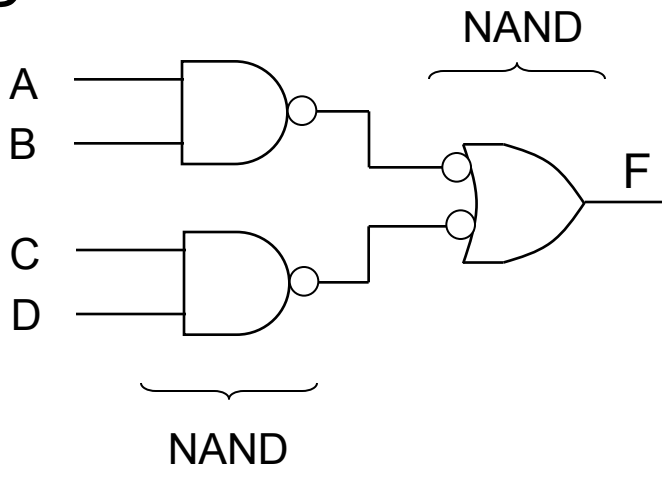
X’+Y’+Z’ = (XYZ)’

AND-NOT = NOT-OR

Implementation using NANDs

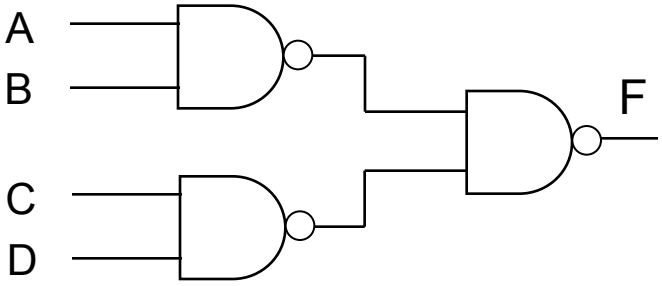
Example: Consider F = AB + CD





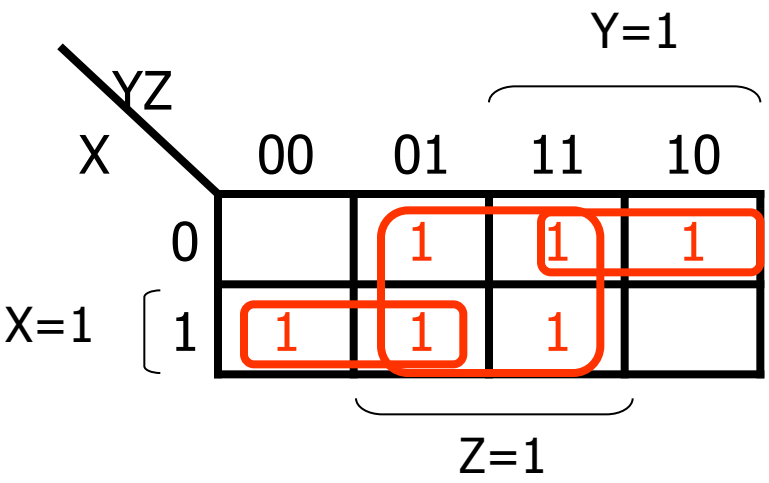
Proof:

$$F = F'' = ((AB)'.(CD)')'$$
$$= ((AB)')' + ((CD)')'$$
$$= AB + CD$$

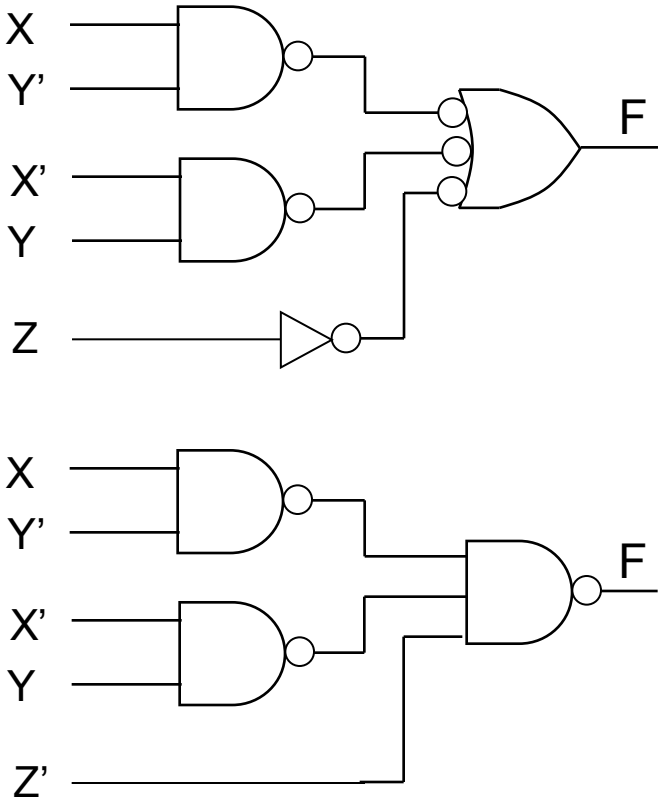


Implementation using NANDs

Consider F =Σm(1,2,3,4,5,7) – Implement using NAND gates



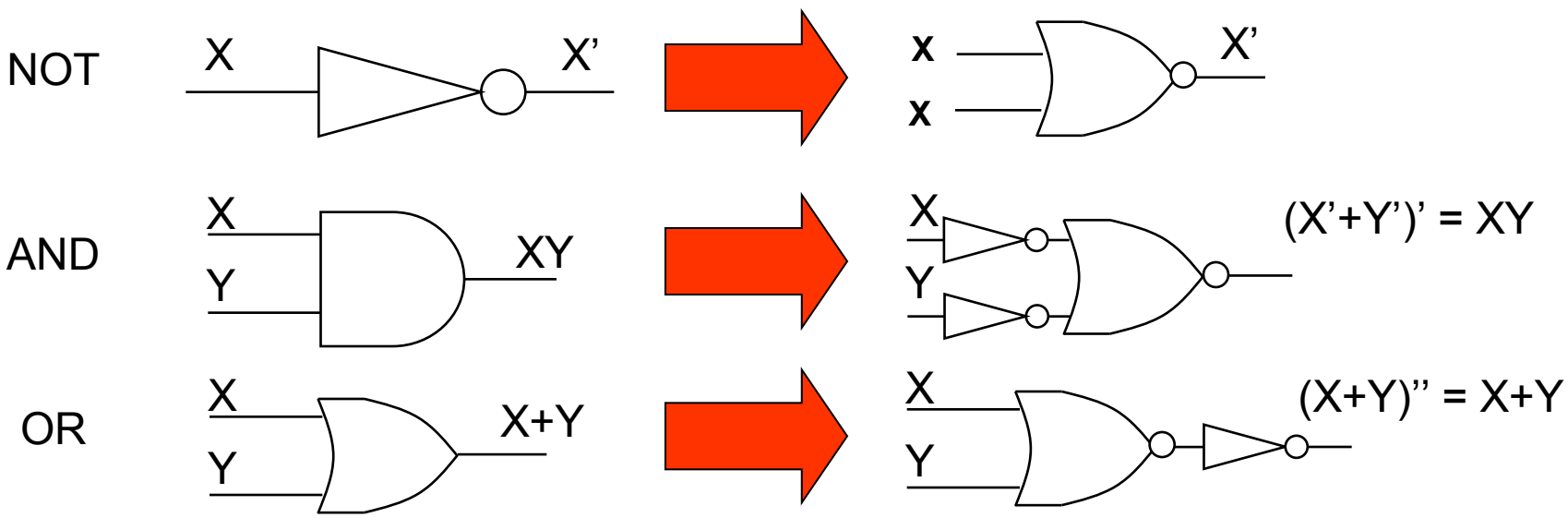
F(X,Y) = Z+XY'+X'Y



Rules for 2-Level NAND Implementations

1. Simplify the function and express it in sum-of-products form
2. Draw a NAND gate for each product term (with 2 literals or more)
3. Draw a single NAND gate at the 2nd level (in place of the OR gate)
4. A term with single literal requires a NOT

NOR Gate is Universal

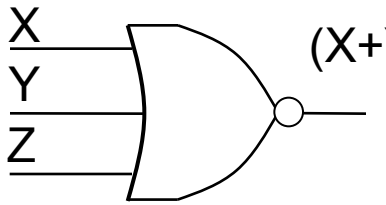


- Therefore, we can build all functions we learned so far using NOR gates ONLY *(Exercise: Prove that NOT can be built with NOR)*
- NOR is a UNIVERSAL gate

Graphic Symbols for NOR Gate

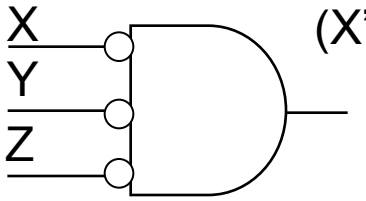
Two equivalent graphic symbols or shapes for the SAME function

OR-NOT



(X+Y+Z)’

NOT-AND

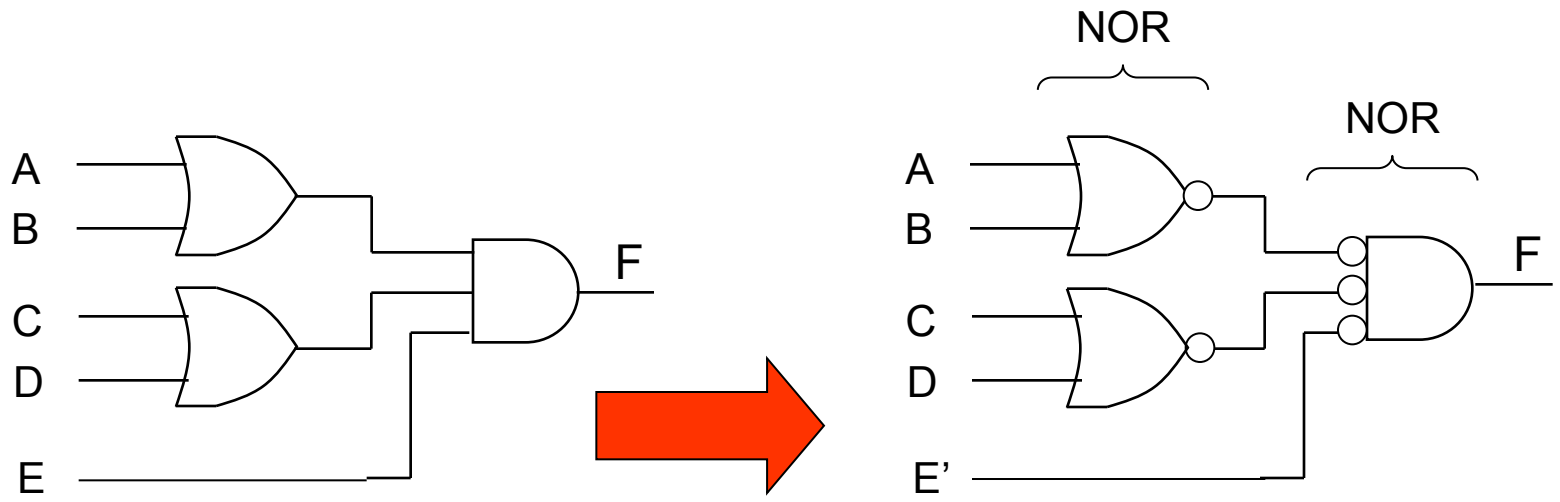


(X’Y’Z’)=(X+Y+Z)’

OR-NOT = NOT-AND

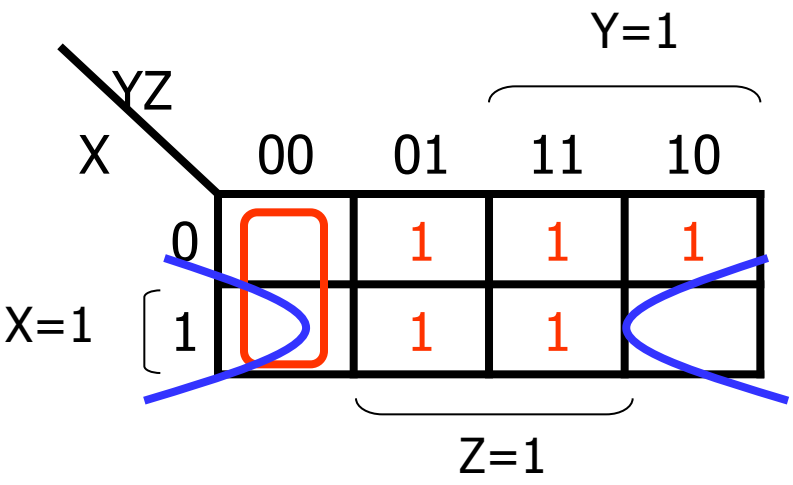
Implementation using NOR gates

Consider F = (A+B)(C+D)E

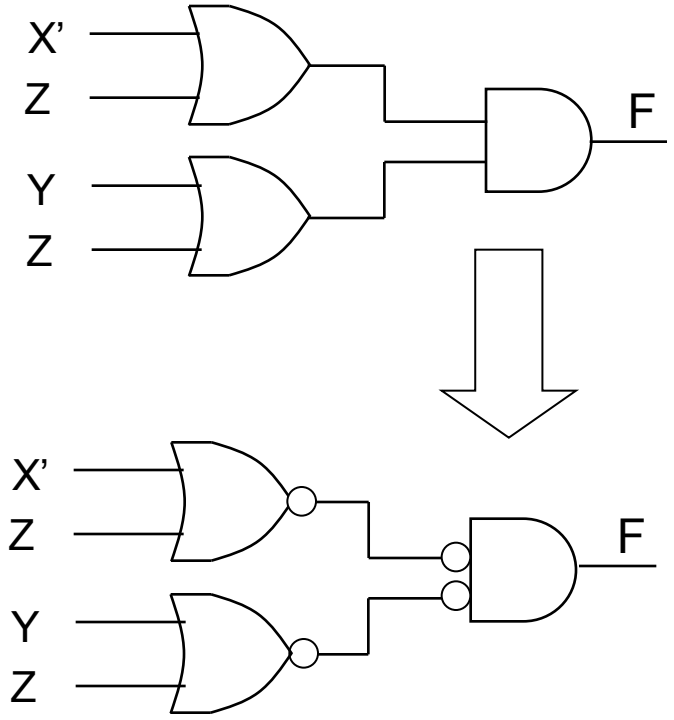


Implementation using NOR gates

Consider F =Σm(1,2,3,5,7) – Implement using NOR gates



F′(X,Y) = Y′Z′+XZ′, or
F(X,Y) = (Y+Z)(X′+Z)



Rules for 2-Level NOR Implementations

1. Simplify the function and express it in product of sums form
2. Draw a NOR gate (using OR-NOT symbol) for each sum term (with 2 literals or more)
3. Draw a single NOR gate (using NOT-AND symbol) the 2nd level (in place of the AND gate)
4. A term with single literal requires a NOT

Reference

1. Moris Mano, “Digital Design With an Introduction to the Verilog HDL”, 5th Edition
2. Ahmad Almulhem, “Digital Design course Slides”, KFUPM 2010